Atomic Layer Deposition: From Development to Commercialization

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Examine Some Case Studies

Where has ALD been successfully commercialized?

What were the critical developments?

What were the critical needs?

How did ALD meet the unmet needs?

Case Studies

1. Electroluminescent & Insulating Layers for Flat Panel Displays
2. High k Gate Dielectrics for MOSFETs
3. Isolation in Magnetic Read Heads
4. Low Leakage, High k Capacitors for DRAM

Thin Film Electroluminescent (EL) Flat Panel Displays

Structure of Thin Film EL Display

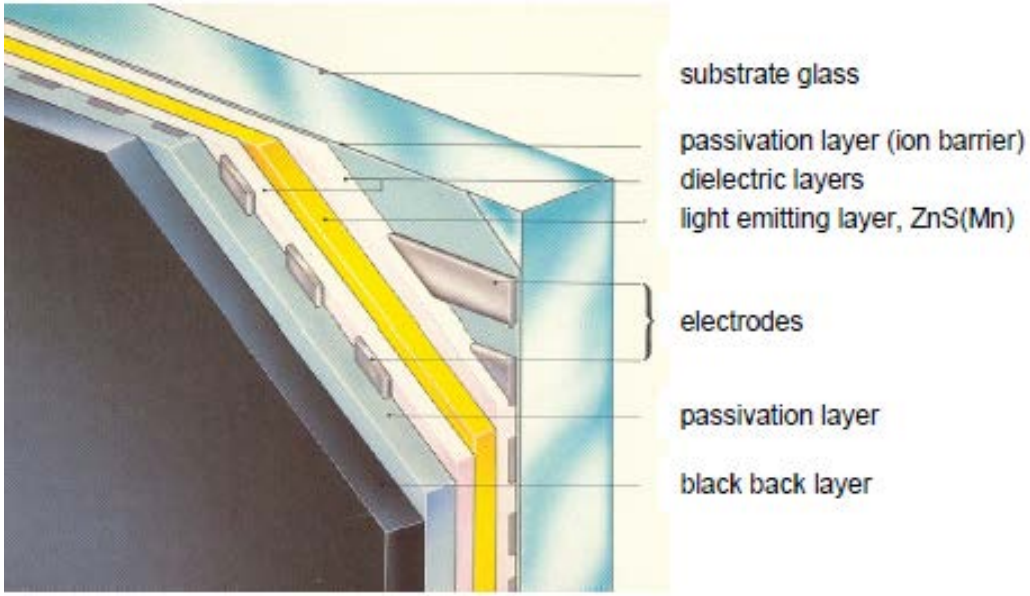
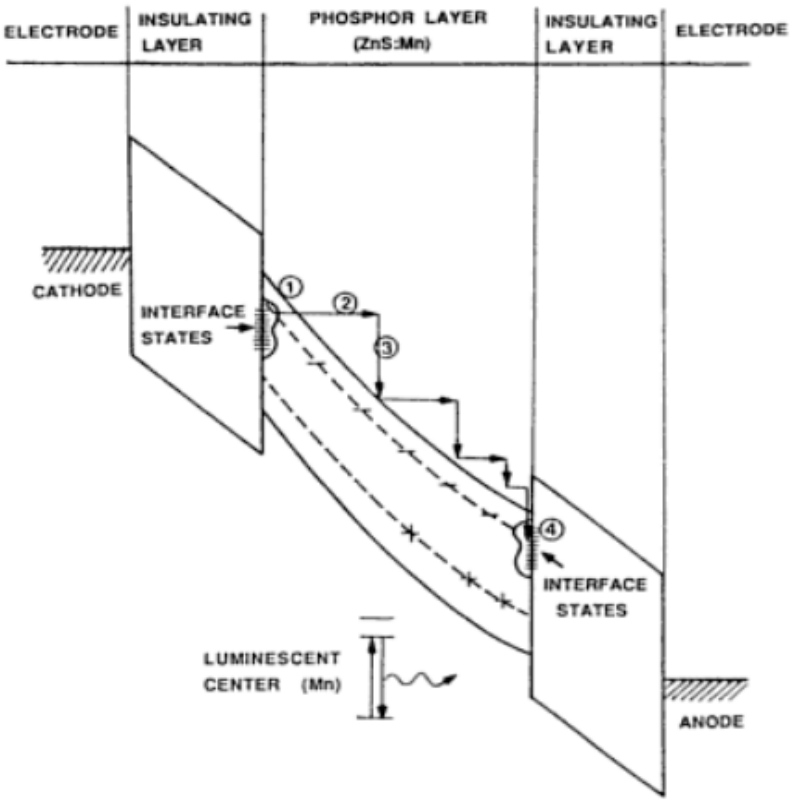


Figure from T. Suntola, ALD2004 in Helsinki

Energy Band Diagram



Needs for EL Flat Panel Display Device

1. Pin-Hole Free, Insulating & Barrier Films
2. High Quality, Thin Luminescent Films
3. Ability to Deposit on Large-Area Substrates

→ Technology in 1970s could not respond to these needs.

→ ALD could meet these needs.

Development of ZnS ALE

First performed by Tuomo Suntola in August/September 1974 as reported by Suntola at ALD2004.

Elemental Precursors | Molecular Precursors

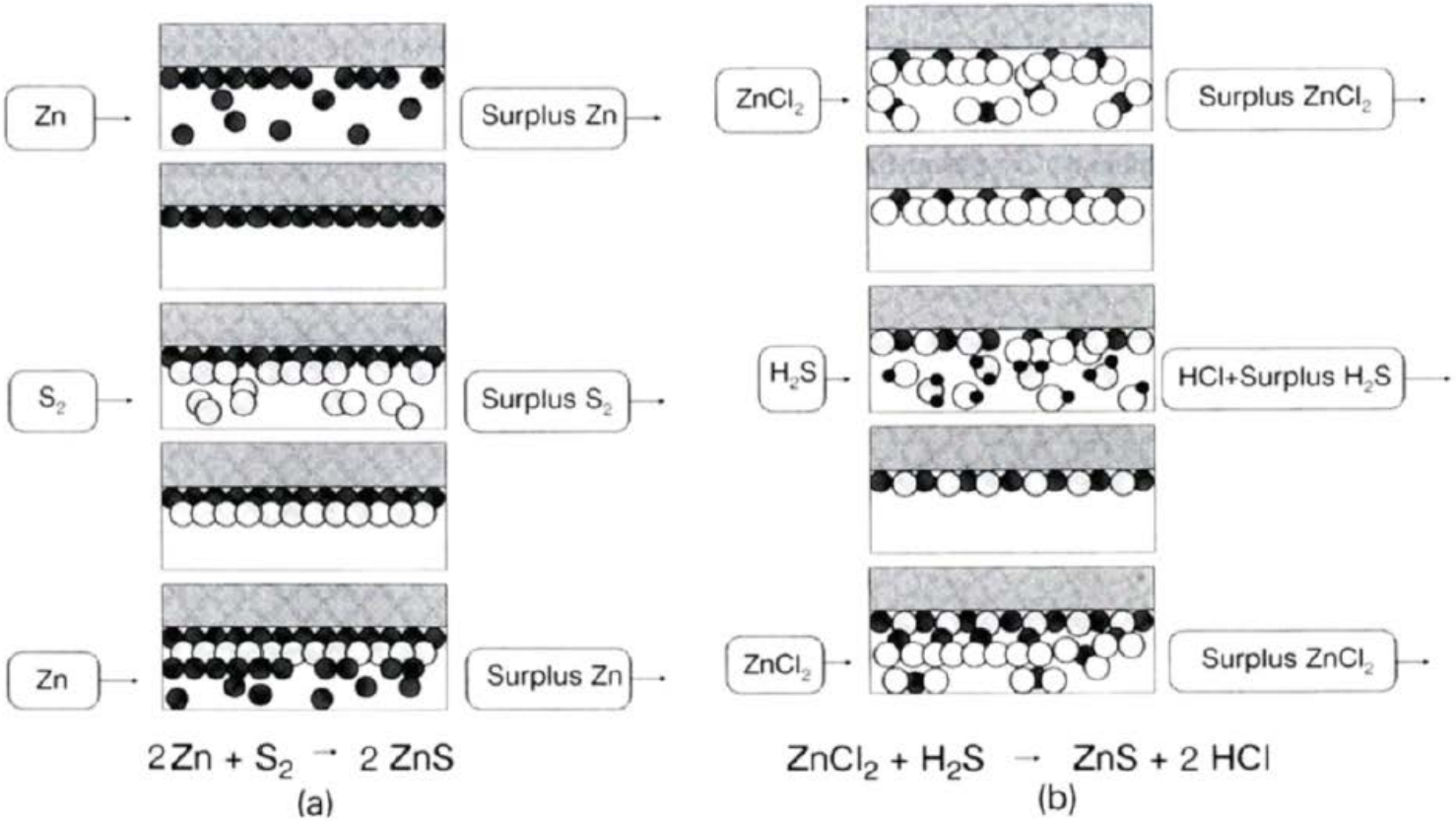
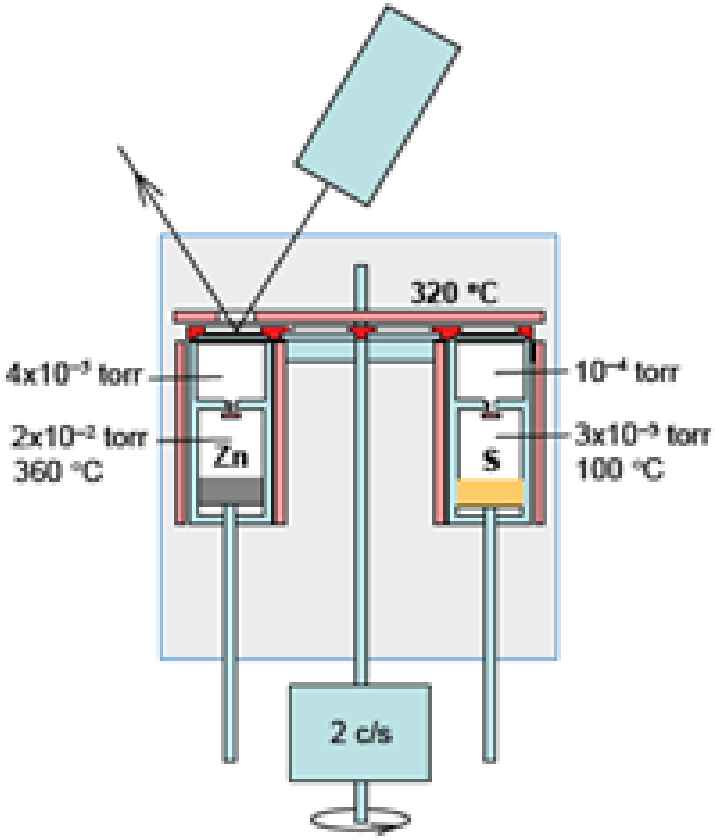


Figure from T. Suntola, *Ann. Rev. Mater. Sci.* **15**, 177 (1985).

Development of ALE Equipment

Equipment for ZnS growth in August/September 1974.



Equipment described in T. Suntola & J. Antson, U.S. Patent #4,058,430 (1977).

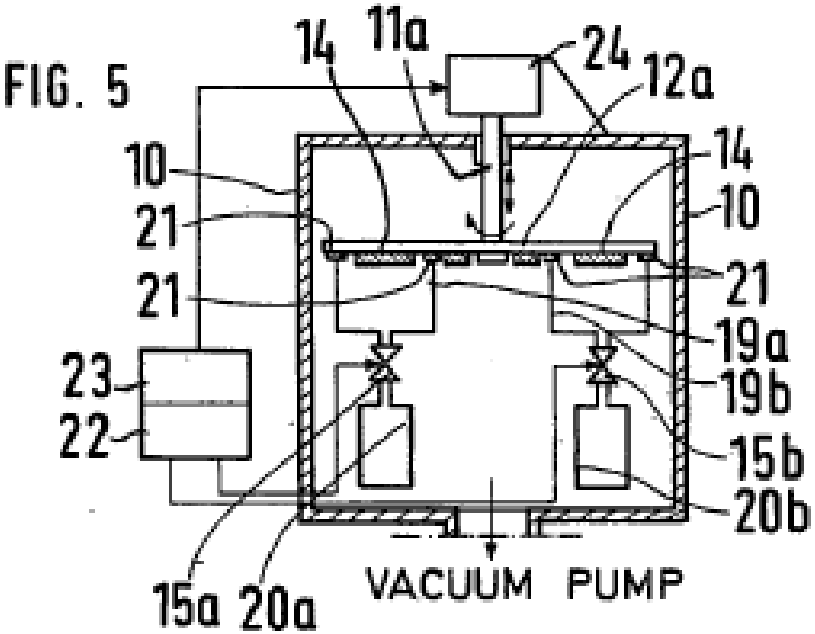


Figure from T. Suntola, ALD2004 in Helsinki

Early Commercialization

First ALD Public Display: EL Display in Helsinki Airport, 1983-1998

Photo from T. Suntola, ALD2004 in Helsinki

Fig. 34. Finlux 640.400 flat panel display.

Finlux, part of Lohja, starts making EL flat panel displays in 1977. T. Suntola leads development project.

Thin Film EL Display Production

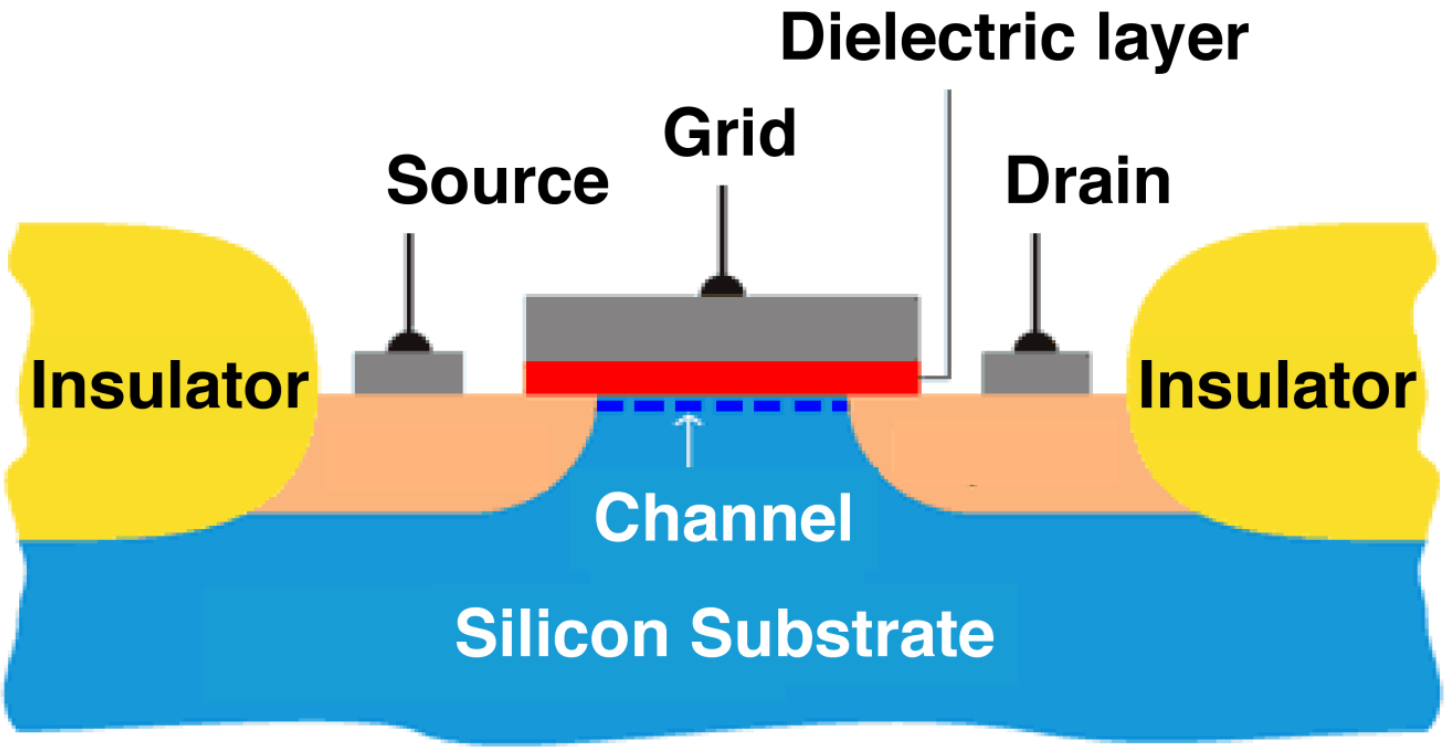
TFEL display manufacturing started in late 1970s and was only application of ALD for ~20 years.

Present Day Thin Film EL Displays from Lumineq (formerly Planar EL Displays). Lumineq is division of Beneq.

Outline

1. Electroluminescent & Insulating Layers for Flat Panel Displays
2. **High k Gate Dielectrics for MOSFETs**
3. Isolation in Magnetic Read Heads
4. Low Leakage, High k Capacitors for DRAM

Gate Dielectric in MOSFET



Metal oxide semiconductor field effect transistor (MOSFET) is main switch used in silicon microprocessors.

Need for High k Gate Dielectric

Miniaturization led to reduction of SiO_2 gate dielectric thickness.

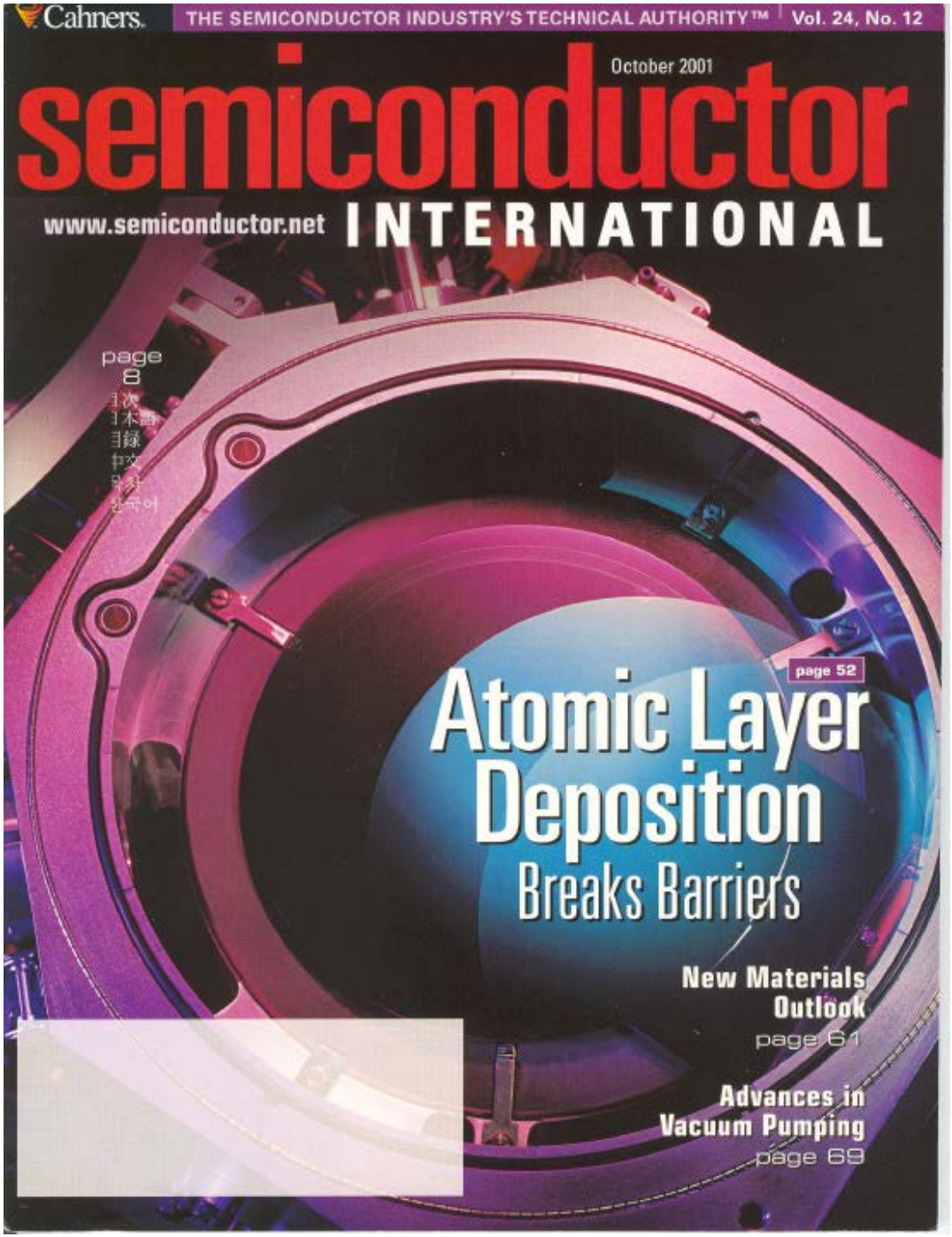
At SiO_2 gate oxide thickness $\leq$ 10 Å, tunneling caused high current leakage.

High k materials were needed to achieve same capacitance with no tunneling.

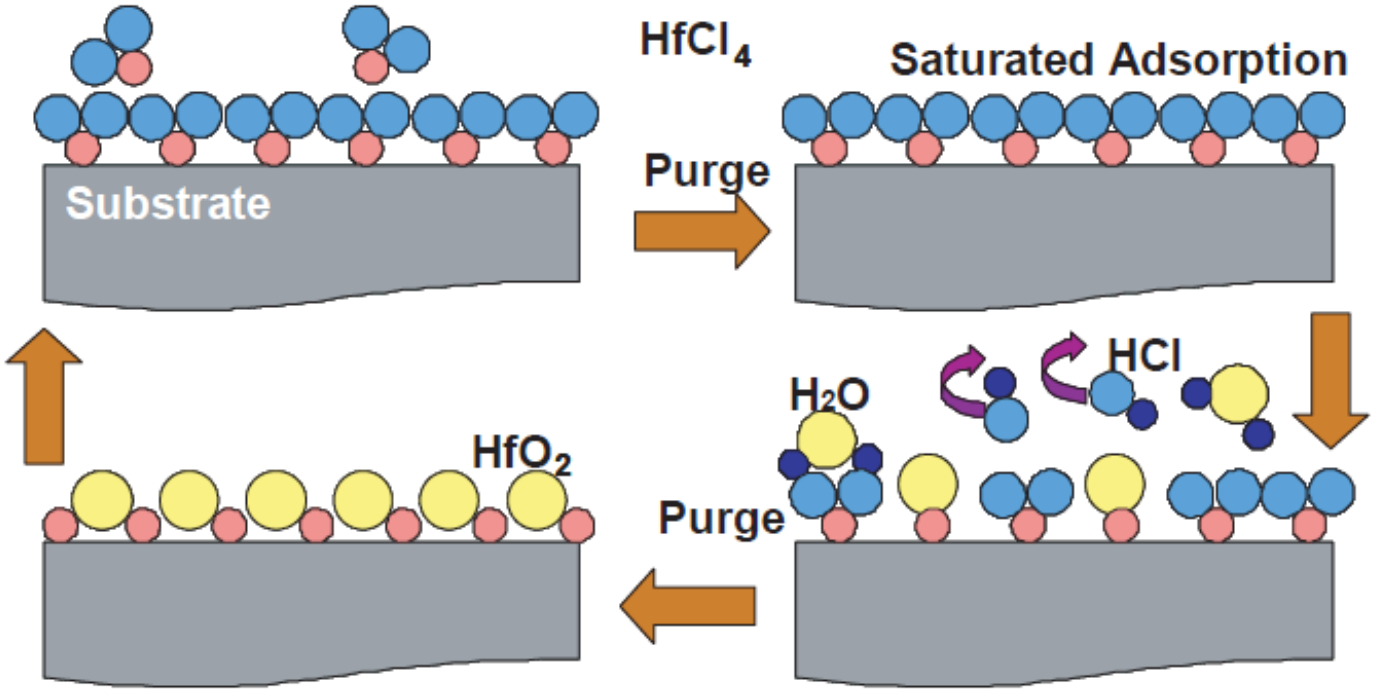
→ **Ultrathin and conformal films of new materials on silicon substrates.**

Cover of *Semiconductor International*, October 2001

Need for ALD for high k gate dielectrics leads to introduction of ALD on International Technology Roadmap for Semiconductors (ITRS).



Development of HfO_2 ALD

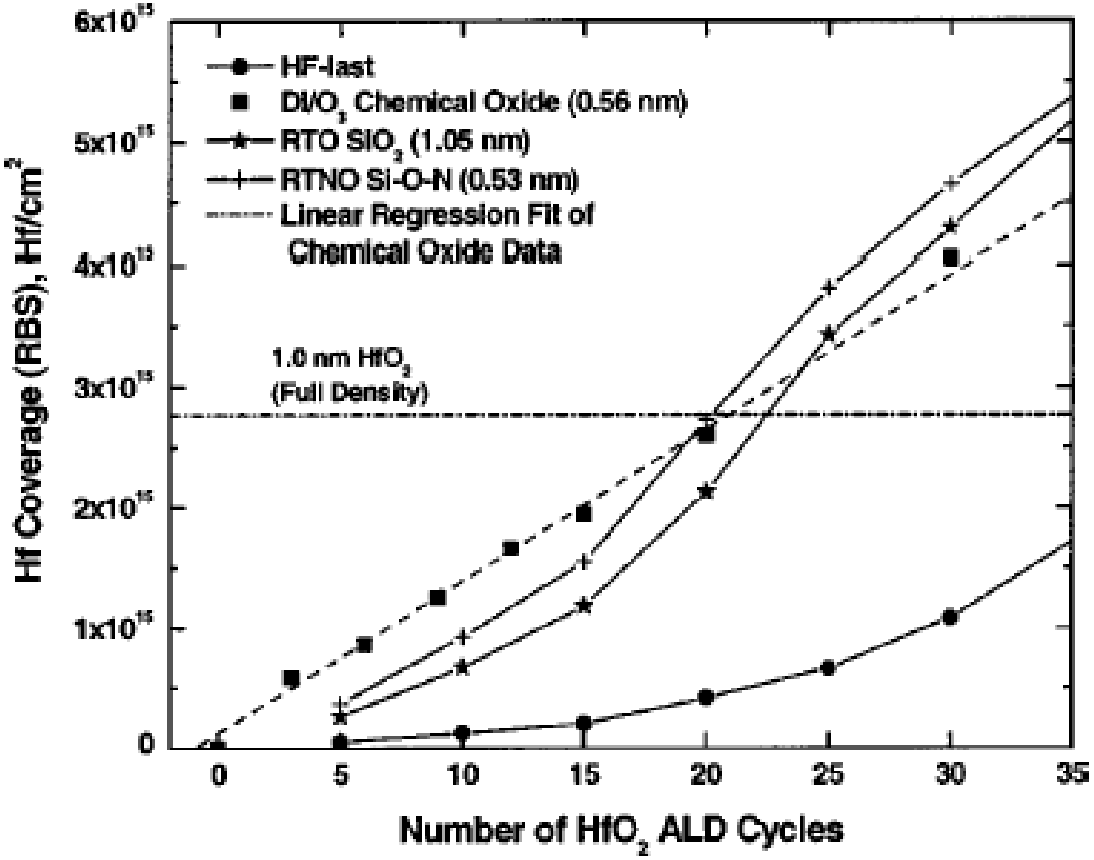


$$HfCl_4(ad.) + 2H_2O(g) \rightarrow HfO_2(s) + 4HCl(g)$$

Chemistry developed by M. Ritala, M. Leskela et al., *Thin Solid Films* **250**, 72 (1994).

Figure from J.P. Chang in *High-k Gate Dielectric Deposition Techniques, High Dielectric Constant Materials* (Springer-Verlag, New York, 2005).

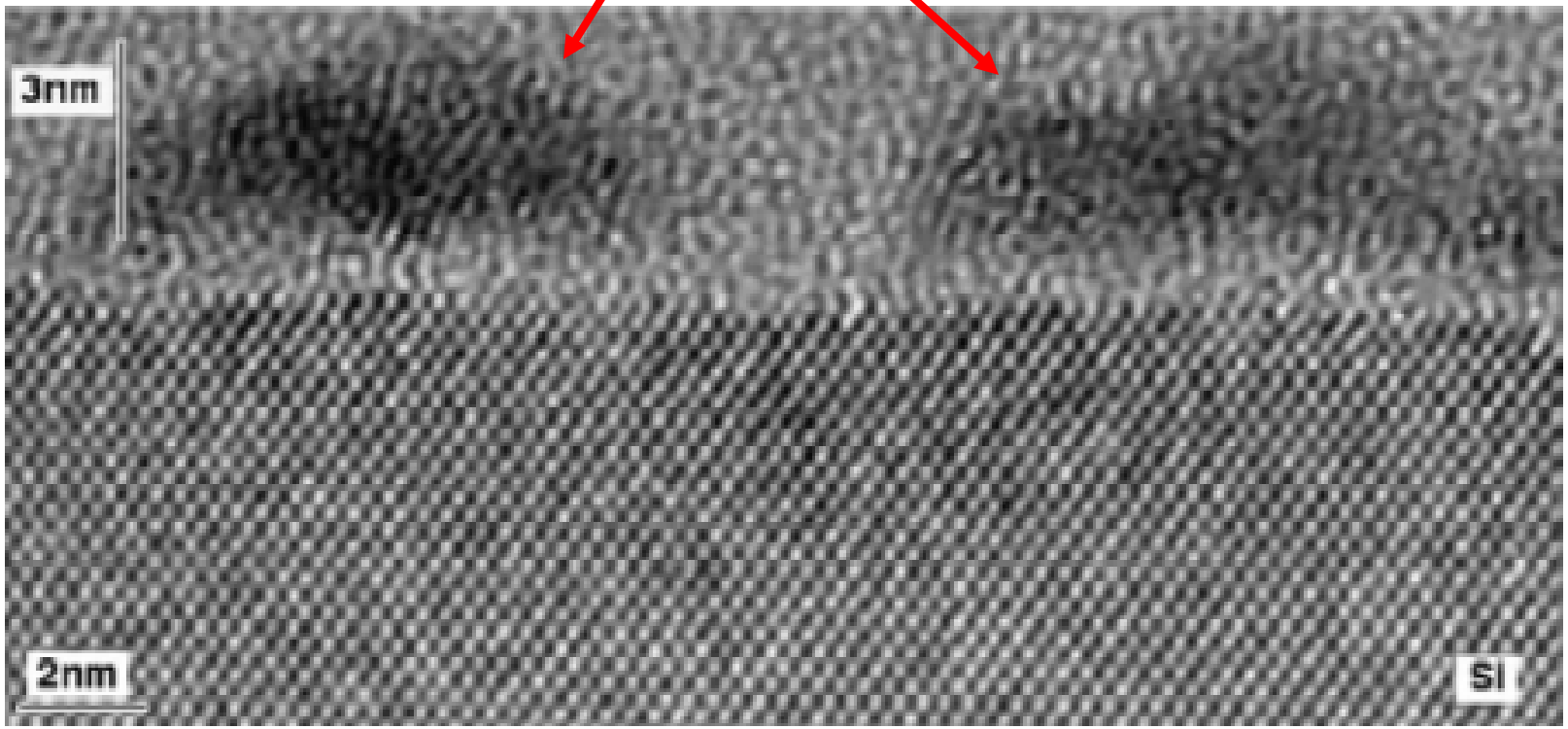
Nucleation Difficulties During HfO_2 ALD on Si(100)



M.L. Green et al., *J. Appl. Phys.* **92**, 7168 (2002).

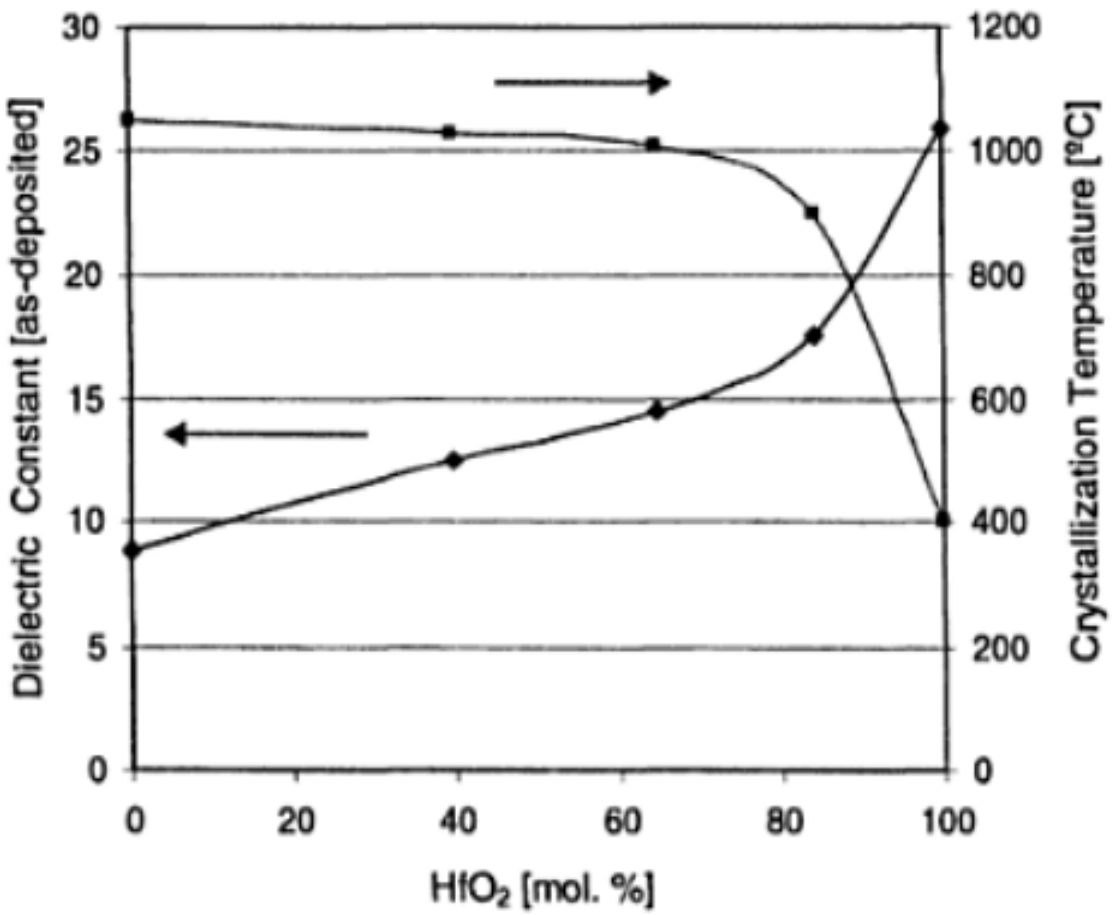
HfO_2 Islands Observed after HfO_2 ALD on H-Si(100)

Islands



E.P. Gusev et al., *Microelect. Eng.* **69**, 145 (2003).

Crystallization Temperature Depends on Al_2O_3 Mole% in HfO_2

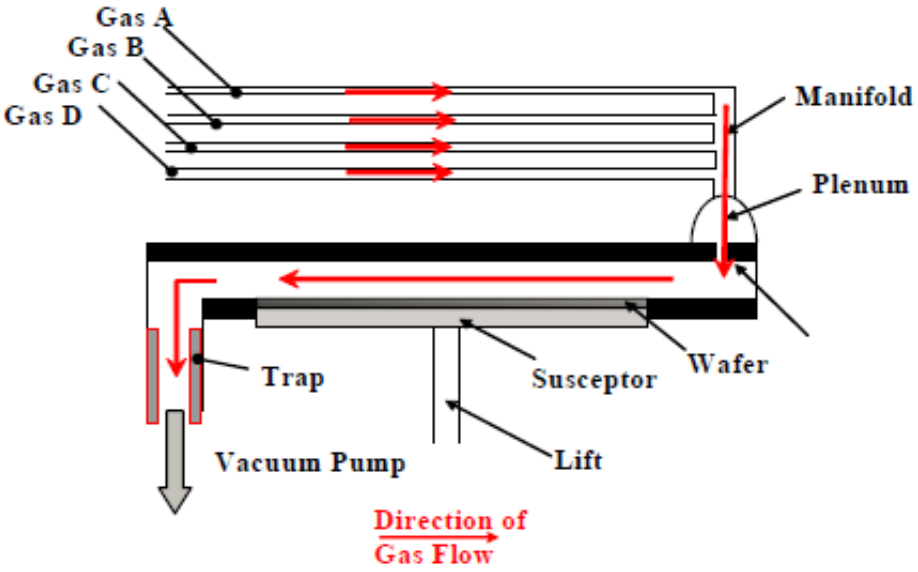


A.R. Londergan et al., ECS Proceedings, Vol. 2002-11, page 163.

Development of ALD Equipment

ASM Pulsar 3000

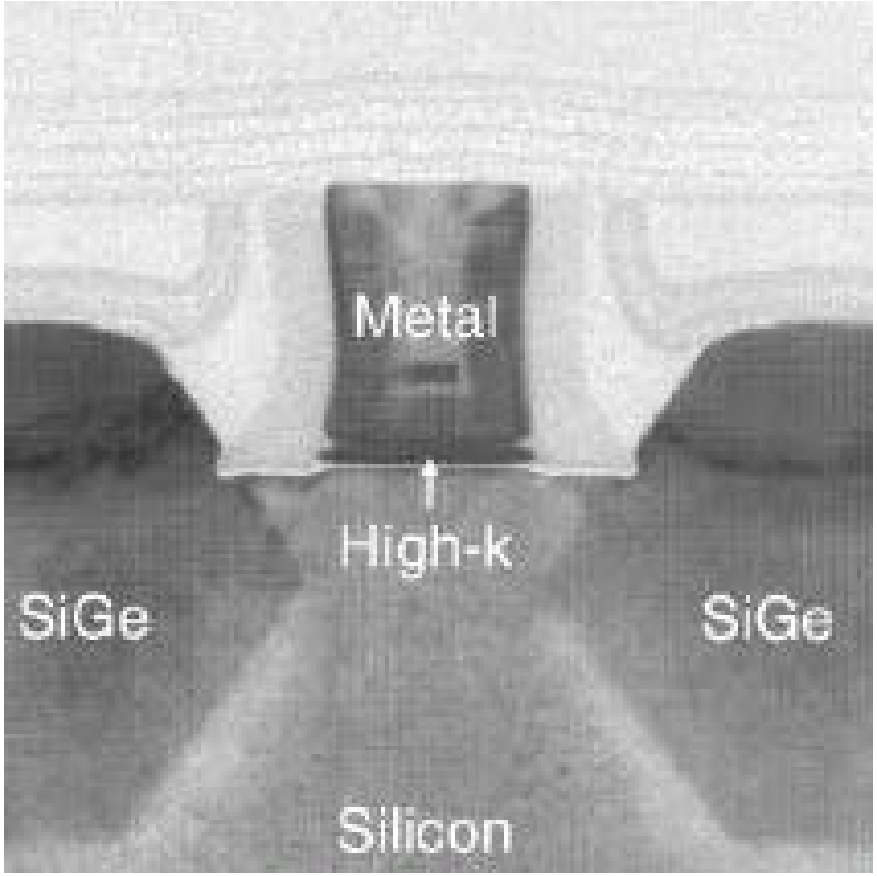
Cross Flow Reactor Design



Figures from Suvi Haukka, ASM Microchemistry, "Role of ALD in Development of Ever-Shrinking Semiconductor Devices", FinNano, September 15-16, 2009.

Initial Commercialization by Intel

High k gate dielectrics introduced by Intel in 2007 for 45 nm CMOS technology.



Hafnium-based high k gate dielectric with SiO_2 equivalent oxide thickness (EOT) of 1.0 nm.

K. Mistry et al., Electron Devices Meeting, 2007. IEDM 2007. IEEE International, p. 247-250.

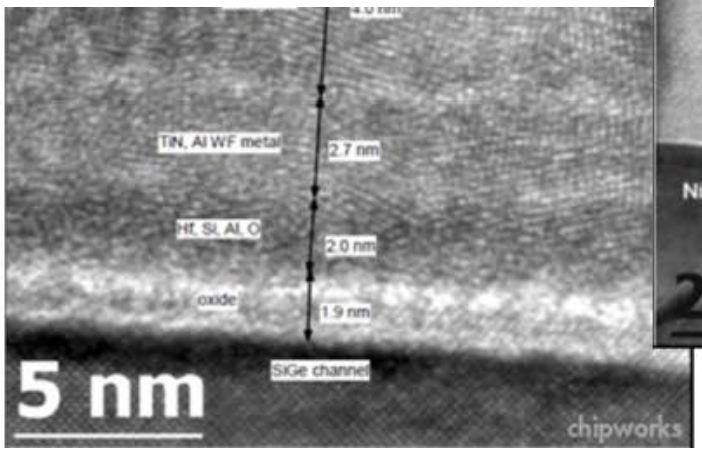
Samsung 32 nm High k Metal Gate PMOS Transistor

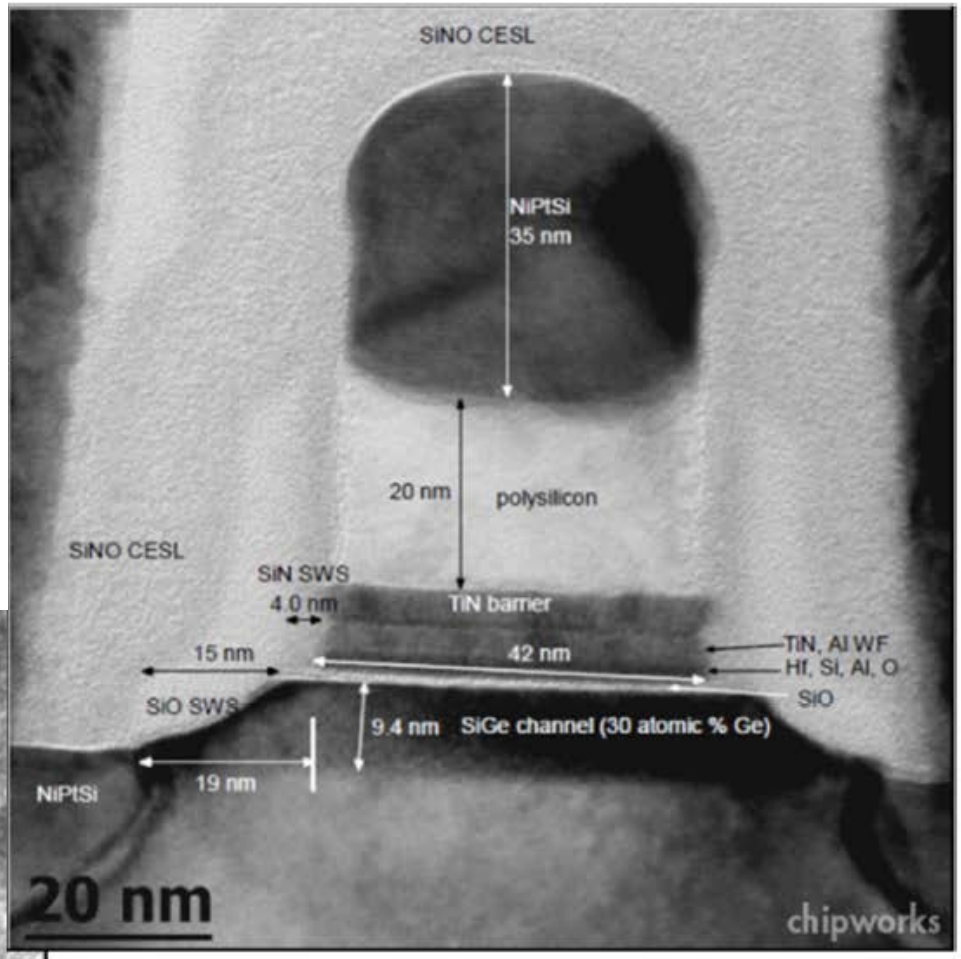
Reverse Engineering by Chipworks

Hf-based high k gate dielectric

Gate oxide thickness ~2.0 nm

TiN metal gate





From Dick James at Chipworks, "Leading Edge Si Devices: an Update"

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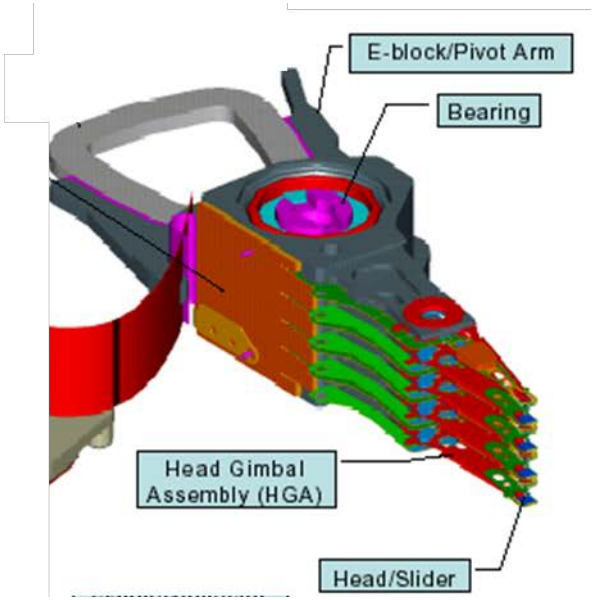
Demanding Needs for Magnetic Isolation in Read Heads



Requirements for Dielectrics:

Breakdown strength > 5 MV/cm
Leakage currents < 10 µA/cm^2 at 1V
Thermal conductivity >1.0 W/mK

Gap Isolation Using Al_2O_3:

Al_2O_3 by PVD
> 50 nm, RF Sputtering
< 50 nm, Reactive Sputtering
Al_2O_3 PVD fails at < 20 nm

Figures and information from M. Kautzky, ALD2003 in San Jose

Linear Growth Rate of Al_2O_3 ALD on NiFe Magnetic Substrate

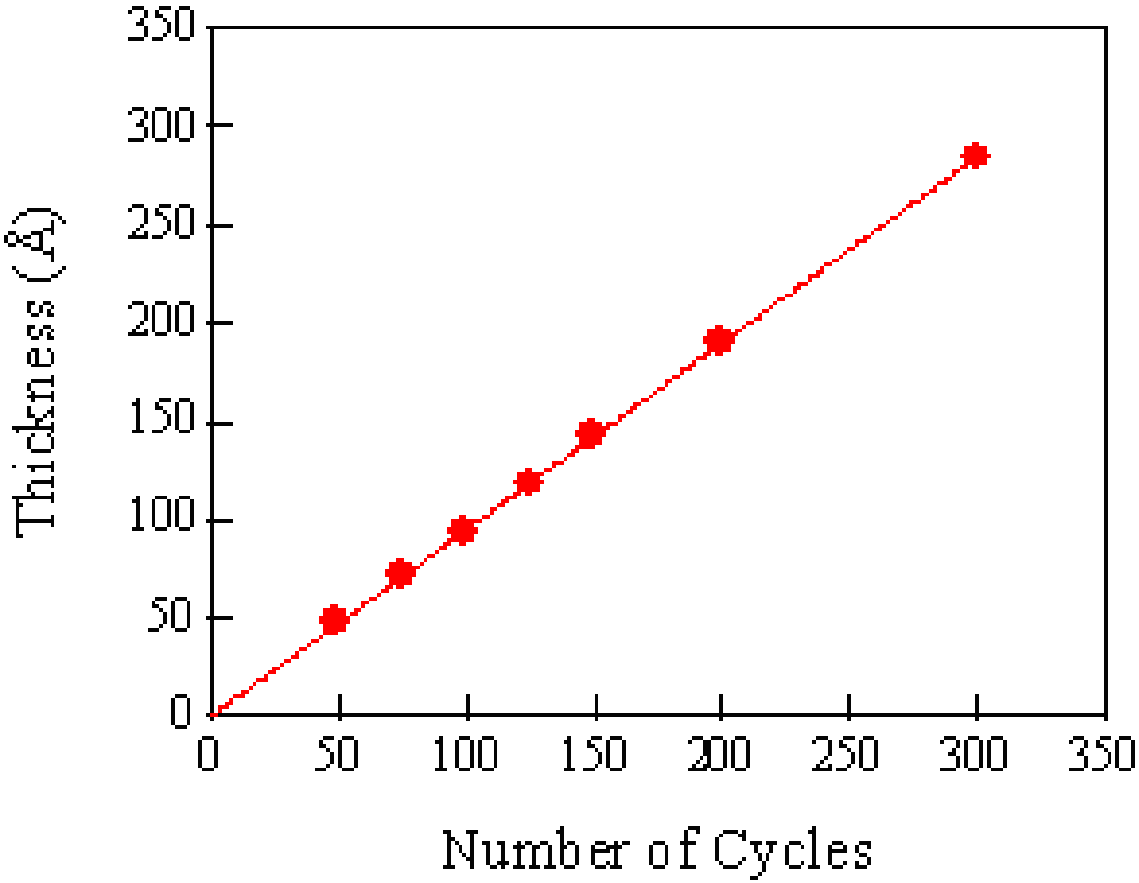
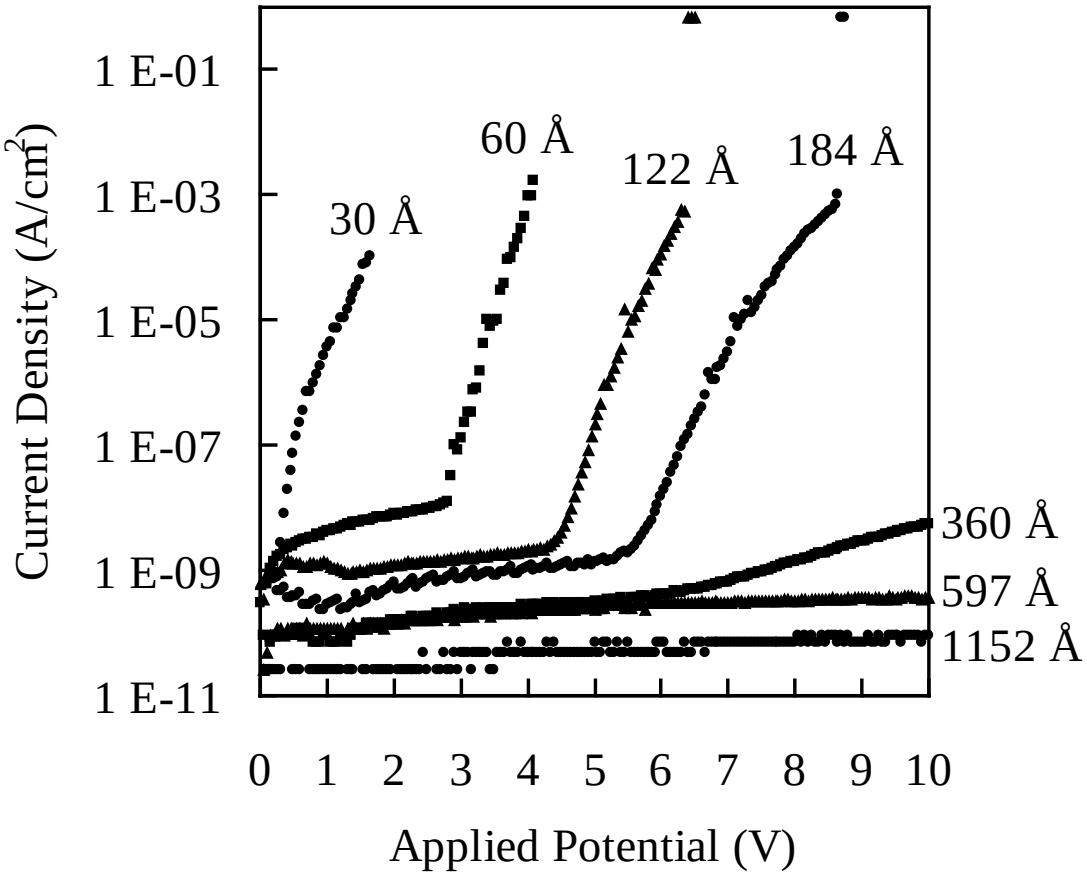


Figure from M. Kautzky, Intermag (2008)

ALD able to provide controlled Al_2O_3 thicknesses at < 20 nm

Current-Voltage Curves for Various Al_2O_3 ALD Film Thicknesses on n-Si(100)



Al_2O_3 ALD Provides Excellent Dielectric Films

Low Leakage. Similar to Thermal SiO_2 Films

M.D. Groner et al., *Thin Solid Films* **413**, 186 (2002).

Performance of Al_2O_3 ALD Led to Rapid Development at Seagate

Device Yield from Al_2O_3 ALD Greatly Exceeded Al_2O_3 from Sputtering

September-October 2000: Tool and Film Evaluations

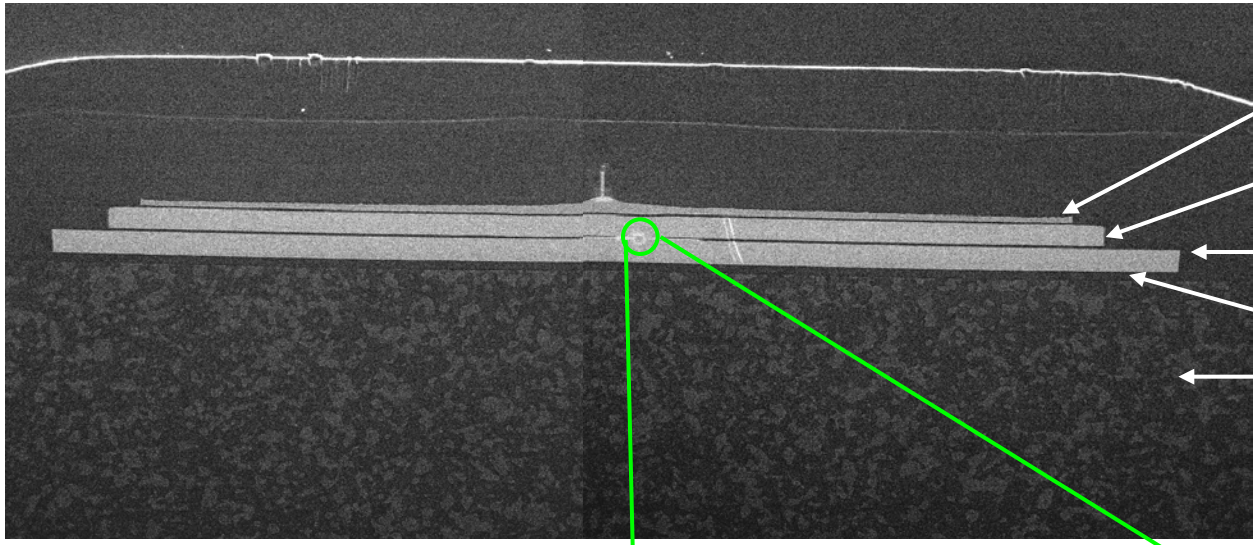
January 2001: Purchase Order for First Tool

April-July 2001: Delivery/ Install/ Qualification of First Tool

Information from M. Kautzky, Private Communication

ALD in Spin-Valve Read Heads

View of Air Bearing Surface



Bottom Pole

Top Shield

Bottom Shield

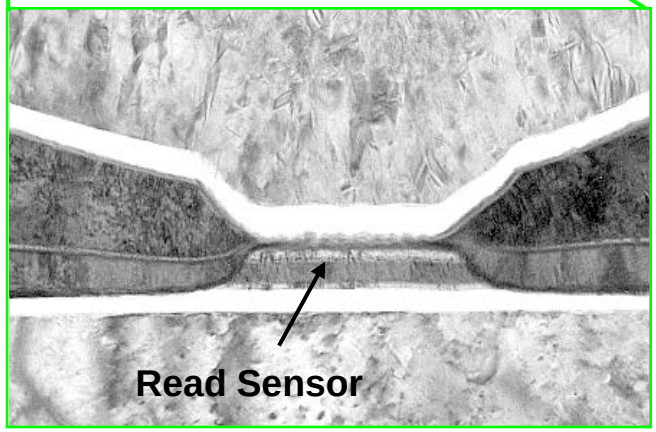
Basecoat

AlTiC substrate

Spin-valve sensor based on "current in plane"

Spin-valve heads in production for 5-6 years

Al_2O_3 ALD thickness ~20 nm



Top Shield

Gap2

Contact

Perm. Magnet

Gap1

Bottom Shield

Figures and information from M. Kautzky, ALD2003 in San Jose

Permanent Magnetic Isolation in Tunneling Magnetic Resistance (TMR) Read Heads

Read heads change from spin-valve to TMR in ~2005

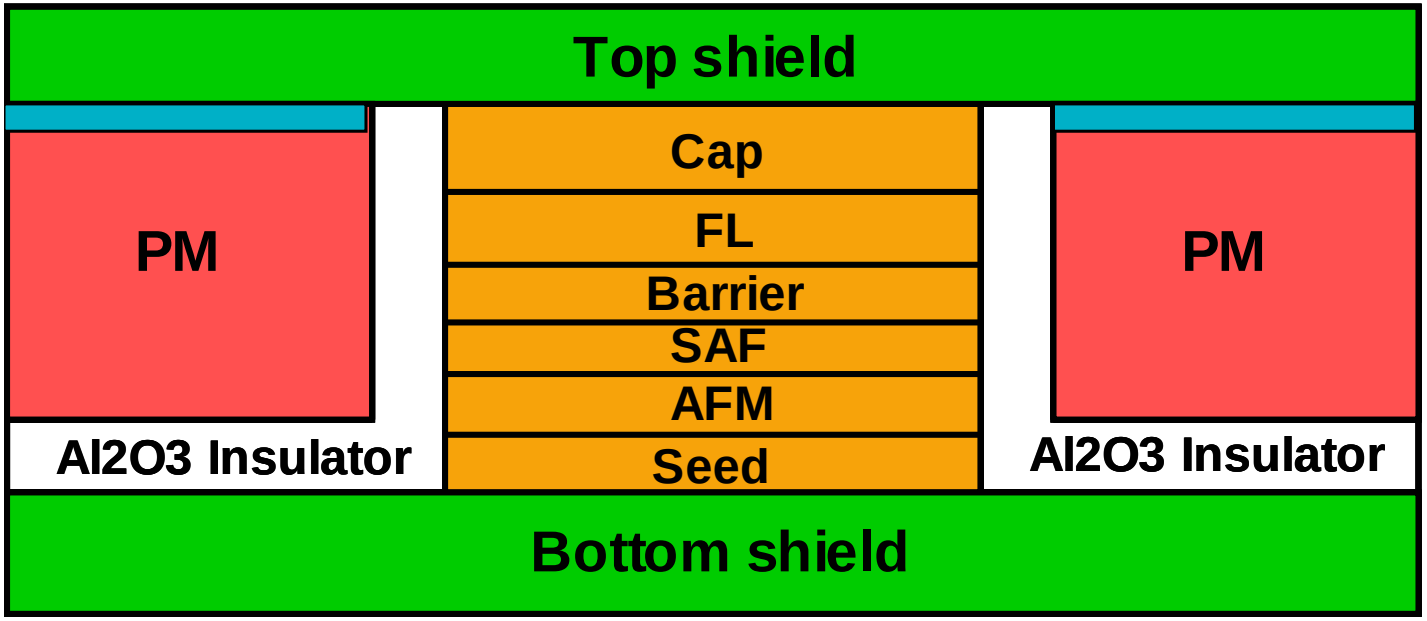
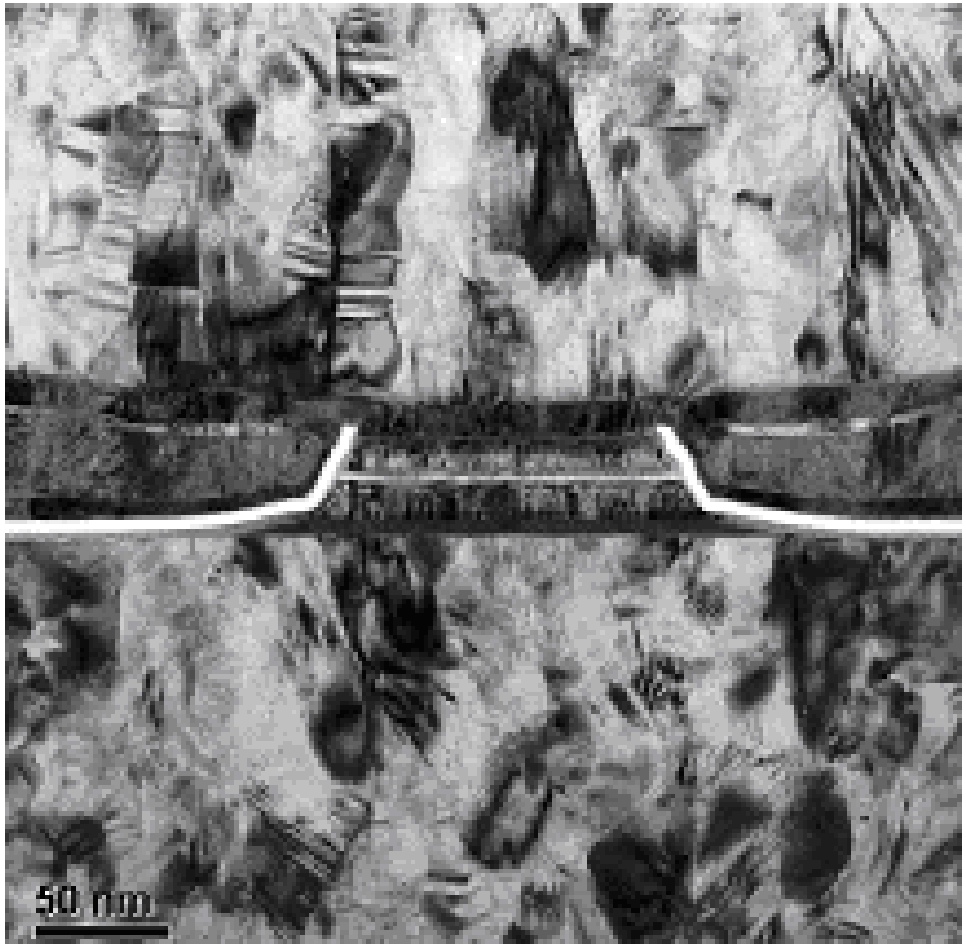


Figure from M. Kautzky, Intermag (2008)

TMR Read with ALD Permanent Magnet Isolation



TMR sensor based on "current perpendicular to plane"

TMR sensor for read width of ~20 nm

Al_2O_3 ALD thickness of ~5 nm

M. Kautzky et al., *IEEE J. Magnetics* **44**, 3576 (2008).

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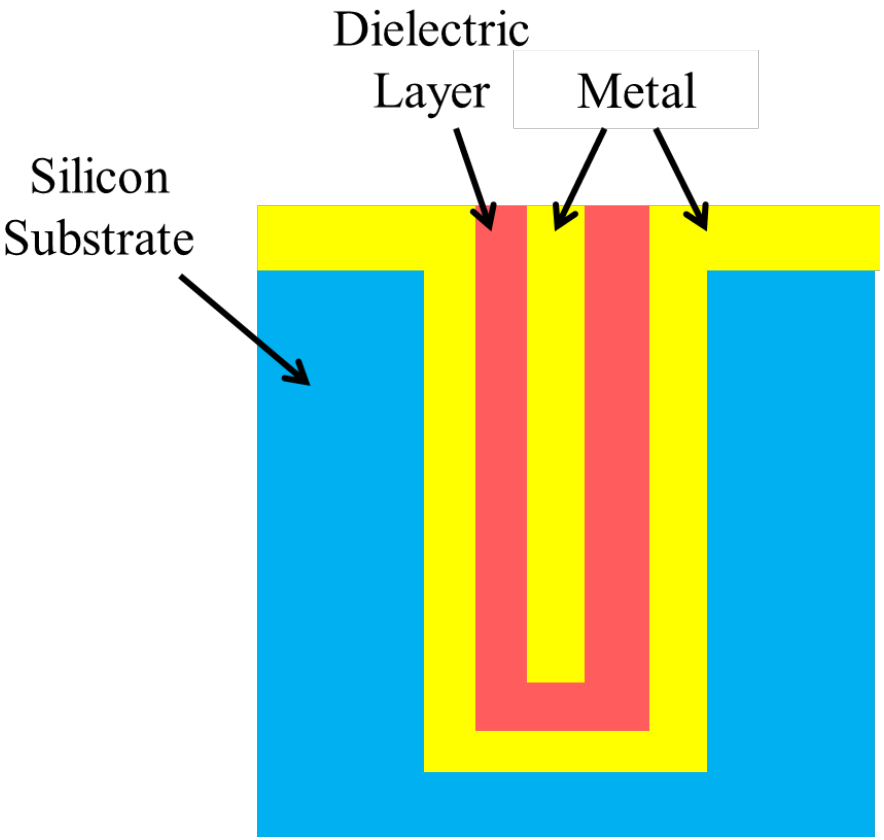
Requirements for Metal-Insulator-Metal (MIM) Capacitors for DRAM

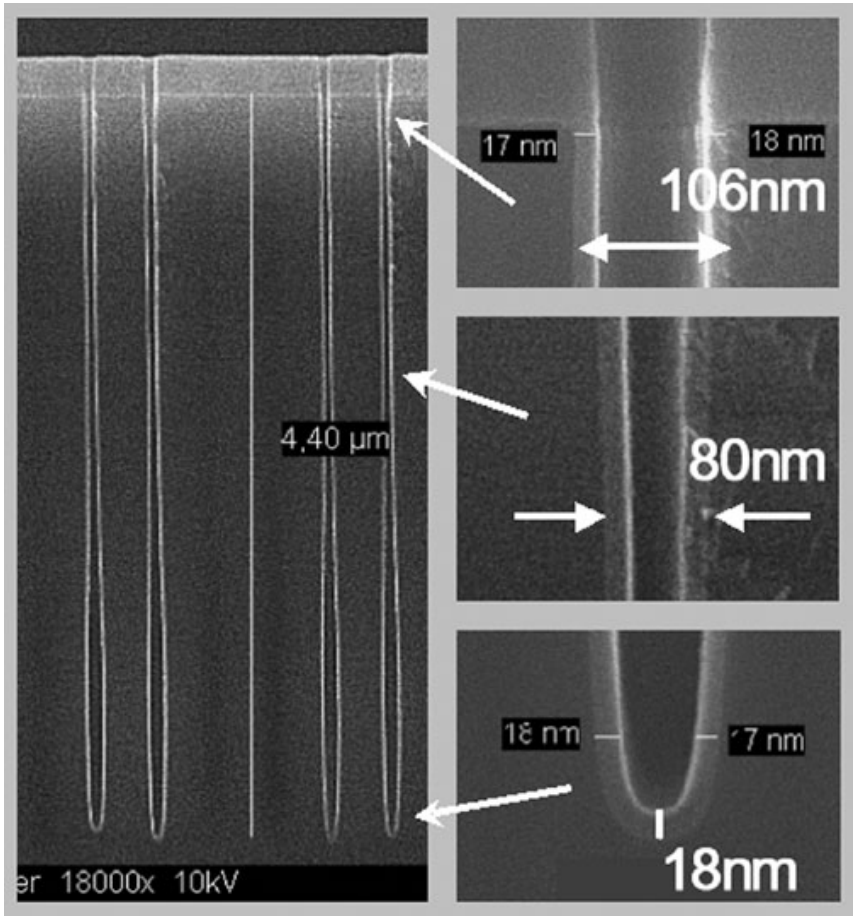


DRAM requires high k dielectric because of miniaturization

Low leakage needed for stable charge storage

Conformality critical because of high aspect ratio structures

ALD Provides Conformality in Trench Capacitor Structures

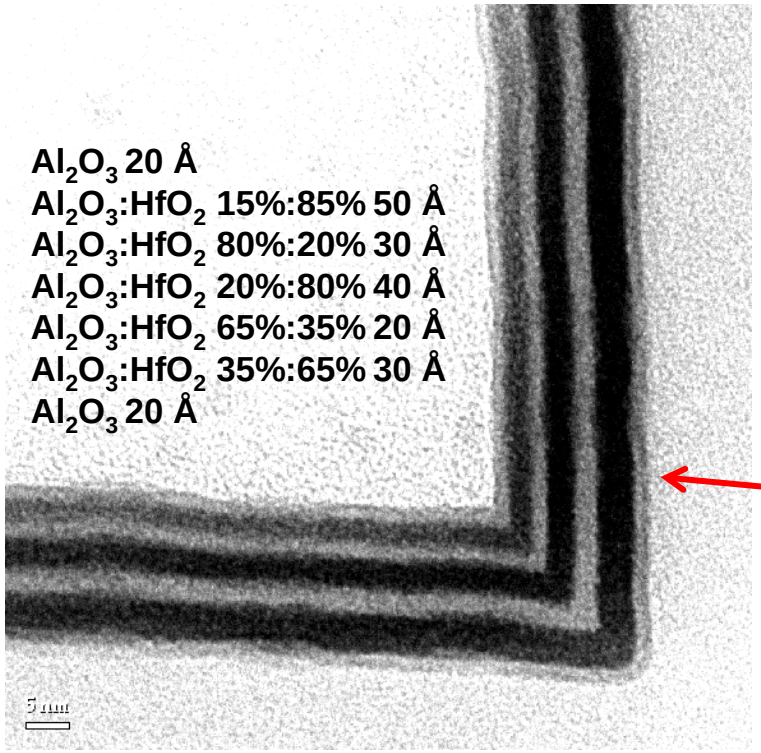


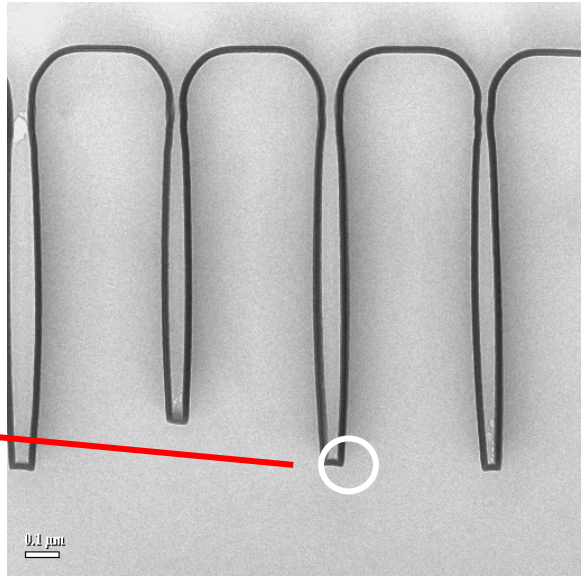
Trench with aspect ratio of ~60 & minimum lateral dimension of ~80 nm

~100% conformality for 18 nm thick Al_2O_3 ALD film

From "Atomic Layer Deposition for Advanced DRAM Applications", Future Fab Intl. Issue 14 (2/11/2003), by M. Gutsche et al. from Infineon Technologies AG

ALD of HfO_2/Al_2O_3 Nanolaminates Yields Low Leakage, High k Insulators





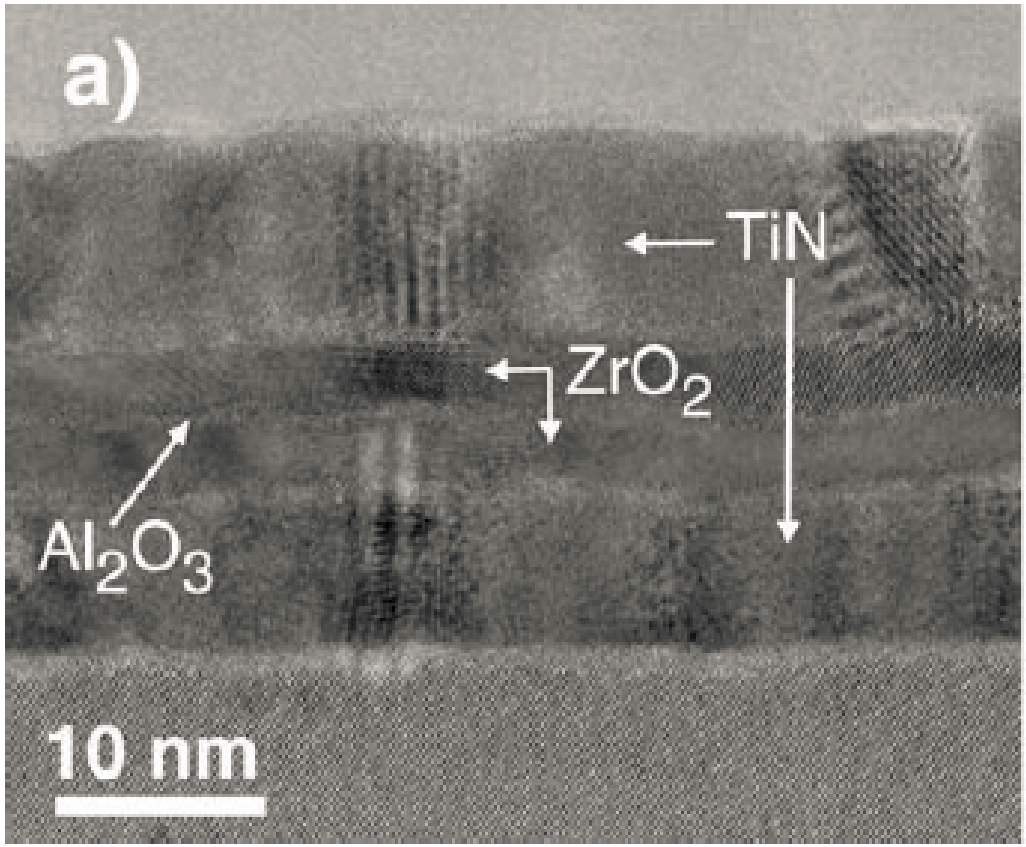
Figures from O. Sneh et al., *Thin Solid Films* **402**, 248 (2002).

ITRS DRAM Roadmap

First year of IC production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
DRAM 1/2 pitch (nm)	52	45	40	36	32	28	25	22	20	18	16	14	13	11	10	8.9
Top electrode	TiN								Ru, RuO_2, Ir, IrO_2							
Capacitor Dielectric Material	ZrO_2, HfO_2, Ta_2O_5								TiO_2, STO, BST							
Bottom electrode	TiN								Ru, RuO_2, Ir, IrO_2					$SrRuO_3$		

Table from *International Technology Roadmap for Semiconductors*, 2009 Edition

DRAM MIMCap Based on TiN/ZAZ/TiN Structure



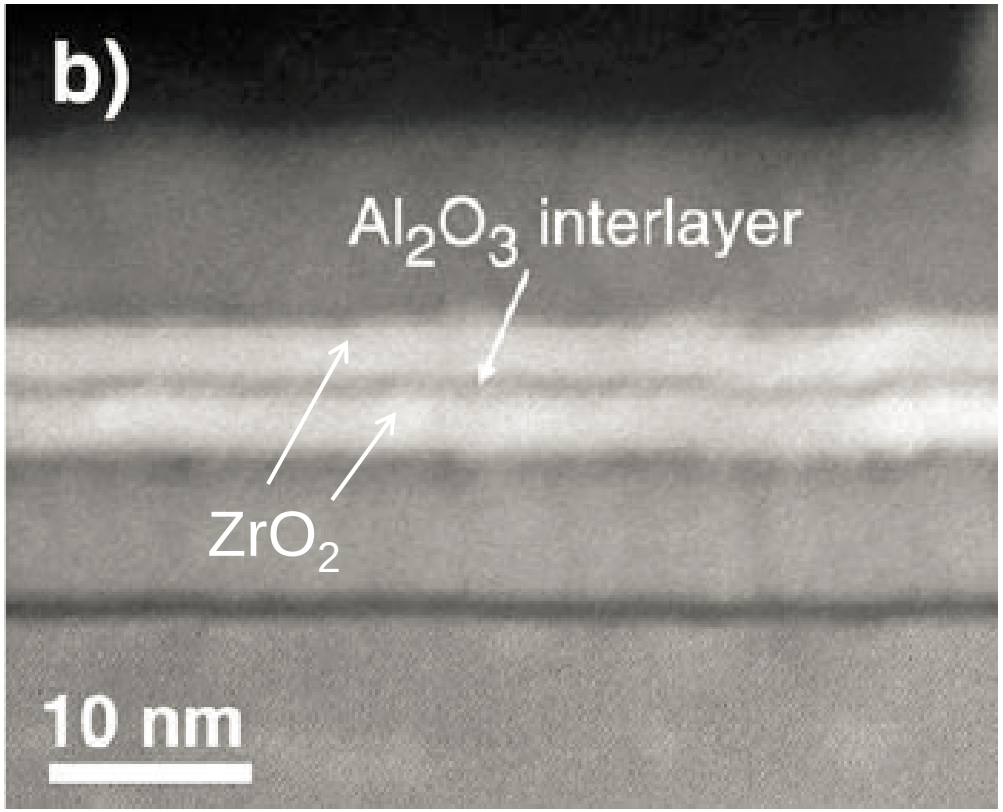
Demonstrated in 2006 by Hynix Semiconductor

ZAZ is tri-layer of $ZrO_2/Al_2O_3/ZrO_2$

TiN, ZrO_2 and Al_2O_3 by ALD

J.A. Kittl et al., *Microelect. Eng.* **86**, 1789 (2009).

STEM Analysis & Performance of ZAZ Stack



Dielectric stack is ~10 nm

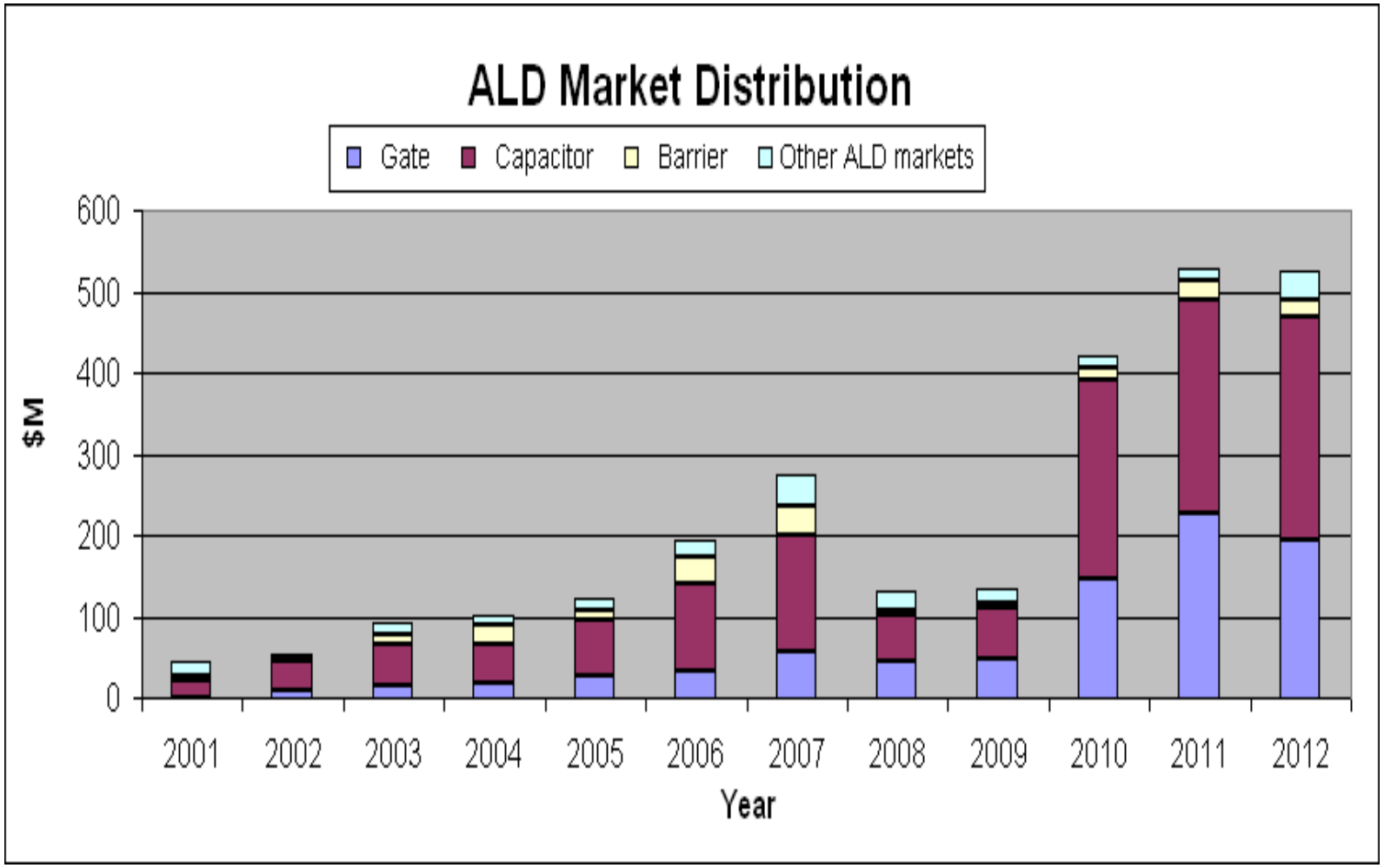
SiO_2 EOT of 0.85 nm

Low leakage of ~10^{-8} A/cm^2 at 1V

J.A. Kittl et al., *Microelect. Eng.* **86**, 1789 (2009).

ALD Semiconductor Equipment Market

Results from VLSI Research, Inc.



Review of Case Studies

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Conclusions from Case Studies

For Successful ALD Applications:

ALD has been able to respond to a critical need when no other method could meet the need.

Future is Promising:

ALD is still moving into fields that are just beginning to appreciate the benefits of ALD.

Additional Developments on Horizon

1. ALD for Passivation of Silicon Wafers
2. ALD on Polymers as Gas Permeation Barriers
3. ALD for Energy Applications
4. ALD for Materials Enhancement

Acknowledgements

ALD in MOSFET and DRAM:

Tom Seidel (formerly Aixtron/Genus)
Michael Current (Current Scientific)
Risto Puhahka (VLSI)

ALD in Magnetic Read Heads:

Mike Kautzky (Seagate)

Other Contributions:

Erwin Kessels (Eindhoven)
Greg Parsons (NC State)